WHAT IS CLAIMED IS:

1. A sensing circuit, comprising:

an integrator to sense charge release from a passive electronic device;

a comparator to interpret the charge release as one of at least two data states;

a compensation module to generate a compensation signal as needed; and

a self-timing module to adjust timing of the integrator sensing based upon a predefined voltage level.

2. The sensing circuit of claim 1, wherein the self-timing module is operable to receive a threshold voltage level and an integration mode identifier.

3. The circuit of claim 2, wherein the threshold voltage level is externally programmed.

4. The circuit of claim 1, wherein the passive electronic device is a ferroelectric memory cell.

5. A timing circuit, comprising:

a voltage generator to generate a threshold voltage signal;

an amplifier to amplify a reference voltage signal; and

a comparator to detect when the reference voltage becomes substantially equal to the threshold voltage and to generate a read out signal.

6. The timing circuit of claim 1, wherein the circuit includes a control module to decode command signal and generate control signals based upon those command signals.

7. The timing circuit of claim 1, wherein the amplifier further comprises a pre-amplifier.

8. The timing circuit of claim 1, wherein the timing circuit further comprises a timeout timer to generate a timeout signal, wherein the timeout signal causes the comparator to generate the read out signal regardless of the level of the reference voltage.

9. The timing circuit of claim 1, wherein the threshold voltage signal is adaptively adjustable.

10. The timing circuit of claim 1, wherein the threshold voltage signal is adjustable by the user.

11. A method for sensing output on a passive electronic device, the method comprising:

predefining a threshold voltage level;

comparing a reference voltage to the threshold voltage level;

generating a read out signal when the reference voltage level becomes substantially equal to the threshold voltage level;

sensing an output voltage level upon reception of the read out signal; and

determining if the output voltage level is one of two data states, producing a first read signal.

12. The method of claim 11, wherein generating a read out signal further comprises receiving a time out signal and generating a read out signal regardless of the reference voltage level.

13. The method of claim 11, wherein the method further comprises repeating the comparing, generating a read out signal, and sensing processes to produce a second read signal.

14. The method of claim 13, wherein determining if the output voltage is one of two data states depends on the first and the second read signals.

15. The method of claim 13, wherein results acquired from the first read signal and the second read signals are subtracted.

16. The method of claim 13, wherein threshold voltage is predefined externally.

17. The method of claim 13, wherein the threshold voltage is adjustable.